

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Kouji MATSUO)
) Group Art Unit:
Serial No.: Not Yet Assigned)
) Examiner:
Filed: September 10, 2003)
)
For: SEMICONDCUTOR DEVICE)
INCLUDING METAL)
INSULATOR)
SEMICONDUCTOR FIELD)
EFFECT TRANSISTOR AND)
METHOD OF)
MANUFACTURING THE SAME)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
MAIL STOP: PATENT APPLICATION

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicant brings to the Examiner's attention the documents listed on attached Form PTO-1449. Except the published and patented documents, copies of the listed documents are attached. Applicant respectfully requests that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

The following are listed on the accompanying PTO-1449 and are in a non-English language:

1. JP 2000-252370 - The relevance of this document is discussed at page three of the specification of the present application.
2. JP 2001-203276 - This document discloses that gate electrode materials are different during n-FET and p-FET. The gate electrode of the n-type MISFET is nitrogen doped TiN and the gate electrode of the p-type MISFET is TiN. The relevance of this document is also discussed in corresponding U.S. Patent No. 6,483,151.

In lieu of a statement of relevance or translation of the listed non-English language document, an English-language abstract of the document setting forth the relevance is enclosed.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicant determines that the cited documents do not constitute "prior art" under United States law, applicant reserves the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

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If there is any fee due in connection with the filing of this Statement, please
charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 10, 2003

By: 

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Enclosures
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3137	Serial No.	
Applicant	Kouji MATSUO		
Filing Date	September 10, 2003	Group:	

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date (Pub. date)	Name	Class	Sub Class	Filing Date if Appropriate
	6,376,888 B1	4/23/2002	Tsunashima et al.			
	6,261,887 B1	7/17/2001	Rodder			
	2003/0143825 A1	(07/31/2003)	Matsuo et al.			
	2002/0037615 A1	(3/28/2002)	Matsuo			
	6,483,151	11/19/02	H. Wakabayashi et al.			

FOREIGN PATENT DOCUMENTS

	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
	2001-203276	7/27/2001	Japan			Yes
	2000-252370	9/14/2000	Japan			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Kouji MATSUO, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, U.S. Serial No.: 10/396,453, filed March 26, 2003.
	Kouji MATSUO et al., "SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME", U.S. Serial No. 09/492,780, filed January 28, 2000.

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce